Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A method of operating a digital tuner, comprising:

amplifying a first number of input signals via a variable gain amplifier, an amplifier gain of the variable gain amplifier being set as a function of an entire carrier multiplex present on the first number of input signals;

digitizing the amplified first number of input signals to create respective streams of digitized input data;

providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation;

providing each per-channel front-end with an input selector coupled to each of the streams of digitized input data; and

configuring each of the per-channel front-ends to process a selected one of the first number of streams of digitized input data.

2. (previously presented) A method of operating a digital tuner, comprising:

providing a first number of A/D converters for digitizing a first number of input signals to create respective streams of digitized input data;

providing each A/D converter with a preceding variable-gain amplifier;

setting an amplifier gain as a function of an entire carrier multiplex present on the input signals;

providing a second number of per-channel front-ends for performing baseband translation and filtering in a digital domain and providing outputs suitable for subsequent demodulation;

providing each per-channel front-end with a respective digital signal scaler coupled to a selected one of the streams of digitized input data;

providing an output of the scaler to subsequent stages of its respective per-channel front-end; and

for each per-channel front-end, dynamically scaling the selected incoming stream of digitized input data as a function of a signal power of a desired carrier to minimize variations in a peak magnitude of the output provided to the subsequent stages.

3. (original) A method of operating a digital tuner, comprising:

providing a first plurality of input signals having a second plurality of symbol rates;

providing a first sampling clock that is a common integer multiple of the second plurality of symbol rates;

digitizing the first plurality of input signals using the first sampling clock to create respective streams of digitized input data;

providing a third plurality of per-channel front-ends, each front-end having a baseband converter, a first decimator, and a matched filter;

operating the baseband converter and the first decimator of each per-channel front-end at the first sampling clock; and

for each per-channel front end, providing a selectively decimated number of samples to each matched filter and operating each matched filter at a selected compatible sampling clock, such that a constant number of symbol samples is output from each matched filter.

4. (previously presented) A digital tuner, comprising:

a first plurality of digitizers operating at a common first sampling rate and providing a first plurality of digitized data streams corresponding to a first plurality of analog inputs;

a second plurality of digital front-ends, each front-end including

selector circuitry for selectable coupling of one of the first plurality of digitized data streams to post-selector processing circuitry of the associated front-end, each selector operating independently of the other selectors,

digital frequency conversion circuitry having a selectable conversion frequency from a predetermined set of conversion frequencies, and

post-conversion circuitry having a selectable decimation factor from a predetermined set of decimation factors, the post-conversion circuitry providing an output suitable for subsequent processing by a digital demodulator; and

wherein configuration of the tuner may select any arbitrary combination of one of the first plurality of analog inputs, one of the set of conversion frequencies, or one of the set of decimation factors.

5. (original) The digital tuner of claim 4, wherein the configuration of the tuner is accomplished programmatically.

6. (original) The digital tuner of claim 4, wherein the configuration of the tuner is accomplished remotely.

7. (original) The digital tuner of claim 4, wherein the configuration of the tuner is accomplished automatically.

8. (original) The digital tuner of claim 4, wherein the configuration of the tuner is accomplished dynamically.

9. (original) The digital tuner of claim 4, wherein the configuration of the tuner is accomplished without involving a human operator.

10. (original) The digital tuner of claim 4, wherein the common first sampling rate is an integer multiple of each decimation factor of the predetermined set of decimation factors.

11. (original) The digital tuner of claim 4, wherein each decimation factor of the predetermined set of decimation factors is an integer sub-multiple of the common first sampling rate.

12. (original) The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as a single stage having a configurable decimation factor selected from a predetermined set.

13. (original) The digital tuner of claim 12, wherein the predetermined set includes decimation factors of 10, 20, 40, 80, and 160.

14. (original) The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which some have a fixed decimation factor and others have a configurable decimation factor.

15. (original) The digital tuner of claim 14, wherein the post-conversion circuitry is implemented using a first stage having a fixed decimation factor and a second stage having a configurable decimation factor selected from a predetermined set.

16. (original) The digital tuner of claim 15, wherein the fixed decimation factor is 10.

17. (original) The digital tuner of claim 15, wherein the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

18. (original) The digital tuner of claim 15, wherein the fixed decimation factor is 10 and the predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

19. (original) The digital tuner of claim 4, wherein the post-conversion circuitry is implemented as multiple stages of which each has a configurable decimation factor.

20. (previously presented) A digital tuner comprising:

a first plurality of digitizers, each digitizer in the first plurality of digitizers being configured to receive a plurality of carrier signals and comprising:

a variable gain amplifier configured to amplify the plurality of carrier signals, the variable gain amplifier being set as a function of the plurality of carrier signals received at the each digitizer, and

an analog-to-digital (A/D) converter operatively coupled to an output of the variable gain amplifier and being configured to receive the amplified plurality of carrier signals and convert the amplified plurality of carrier signals to a digital stream of data; and

a second plurality of receiver front-ends, each receiver front-end of the second plurality of receiver front-ends comprising:

a scaler configured to receive a digital stream of data and dynamically scale the digital stream of data to an essentially same peak magnitude.

21. (previously presented) The digital tuner of claim 20 wherein a number of digitizers in the first plurality of digitizers differs from a number of receiver front-ends in the second plurality of receiver front-ends.

22. (previously presented) The digital tuner of claim 20 wherein each receiver front-end further comprises:

a baseband converter operatively coupled to the scaler and being configured to receive the scaled digital stream of data and digitally down-convert the scaled digital stream of data to baseband orthogonal component streams.

23. (previously presented) The digital tuner of claim 22 wherein each receiver front-end further comprises:

a plurality of filtering and decimation pipelines operatively coupled to the baseband converter and being configured to receive the baseband orthogonal component streams and process the received baseband orthogonal component streams.

24. (previously presented) The digital tuner of claim 20 wherein each receiver front-end of the second plurality of receiver front-ends comprises:

a plurality of clock domains comprising a first clock domain operating at a first rate and a second clock domain operating at a second rate.

25. (previously presented) The digital tuner of claim 24 wherein the second rate is a sub-multiple of the first rate.

26. (previously presented) The digital tuner of claim 24 wherein the second rate is selectable.

27 - 29. (canceled)